epitaxial layer from said first region to said second region when the first junction is directly biased, said isolating element comprising a dielectric material adjacent said epitaxial layer and polycrystalline silicon spaced apart from said epitaxial layer by said dielectric material, said isolating element also terminating above a bottom surface of said substrate.

17. (Amended) An integrated structure comprising:

a substrate having a first conductivity type;

an epitaxial layer on said substrate and having the first conductivity type and a conductivity less than a conductivity of said substrate;

first and second regions in said epitaxial layer each having a second conductivity type opposite the first conductivity type, said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and a second junctions therewith; and

an isolating element positioned between said first and said second regions and extending from the surface of said epitaxial layer at least as far as a top surface of said substrate, said isolating element partially surrounding at least one of said first and second regions, said isolating element also terminating above a bottom surface of said substrate.

22. (Amended) An integrated structure formed on a semiconductor chip and comprising:

a substrate having a first conductivity type;

an epitaxial layer on said substrate and having the first conductivity type and a conductivity less than a conductivity of said substrate;